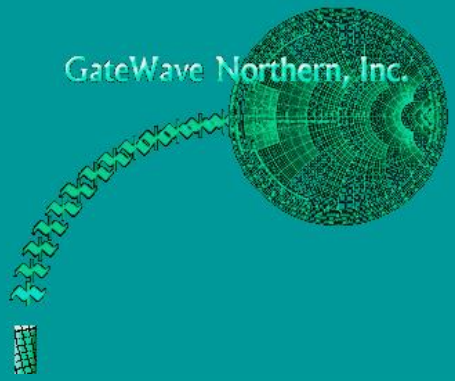
GateWave Northern

Test Results

DUT Electronics PCB/interposer



11/23/22

GateWave Northern, Inc.
6200 Gisholt Dr. Ste. 205
MADISON,WI 53713 USA
608-224-1250
g.hohenwarter@gatewave.com

Objective

- Test PCB/connector characterization
  - 2-port S-parameters for model generation
  - TDR responses

Setup

- Agilent HP8722C VNA option 10
- 50 MHz-40.05 GHz
- Effective risetime ~ 25 ps

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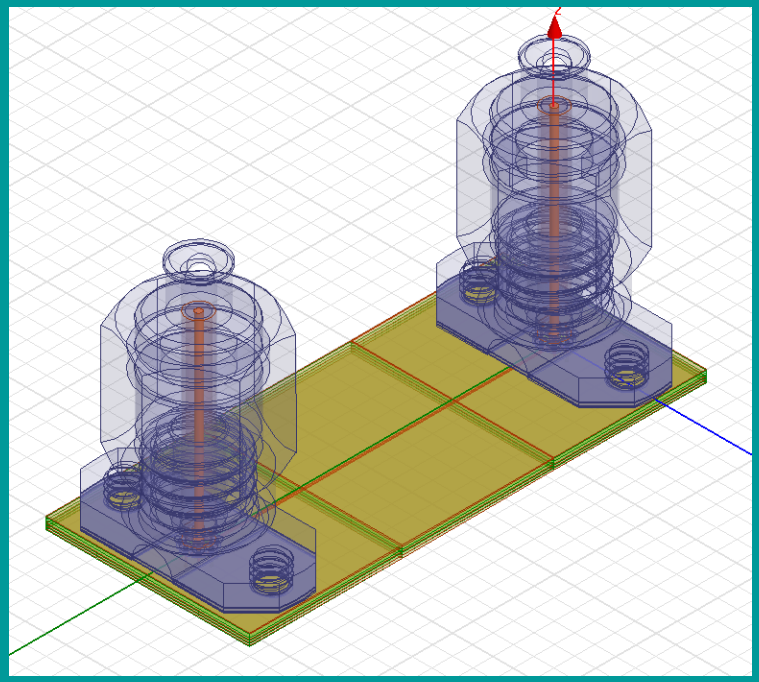
Connections



Test uses DUT electronics 047 interposer and connectors

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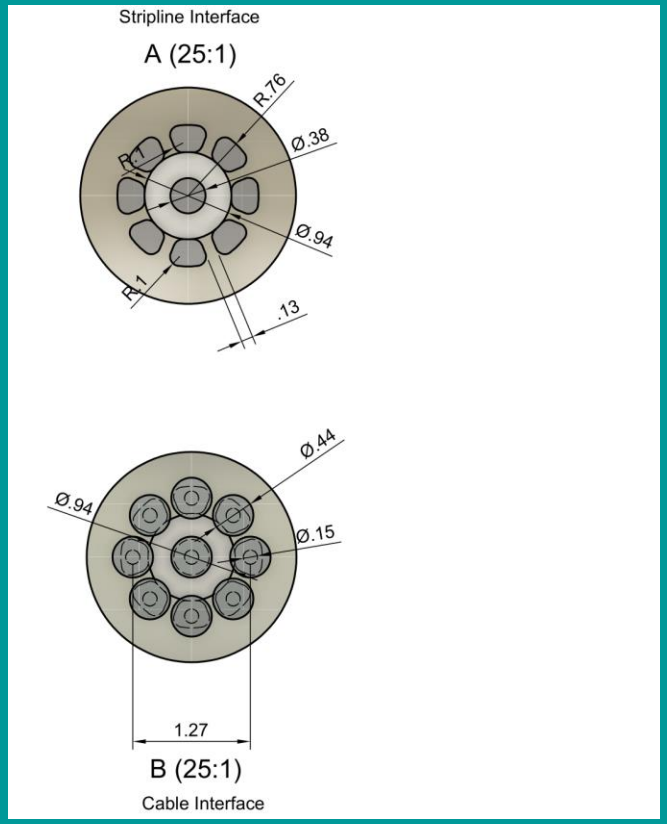
Interposer orientation



Test uses DUT electronics 047 interposer and connectors

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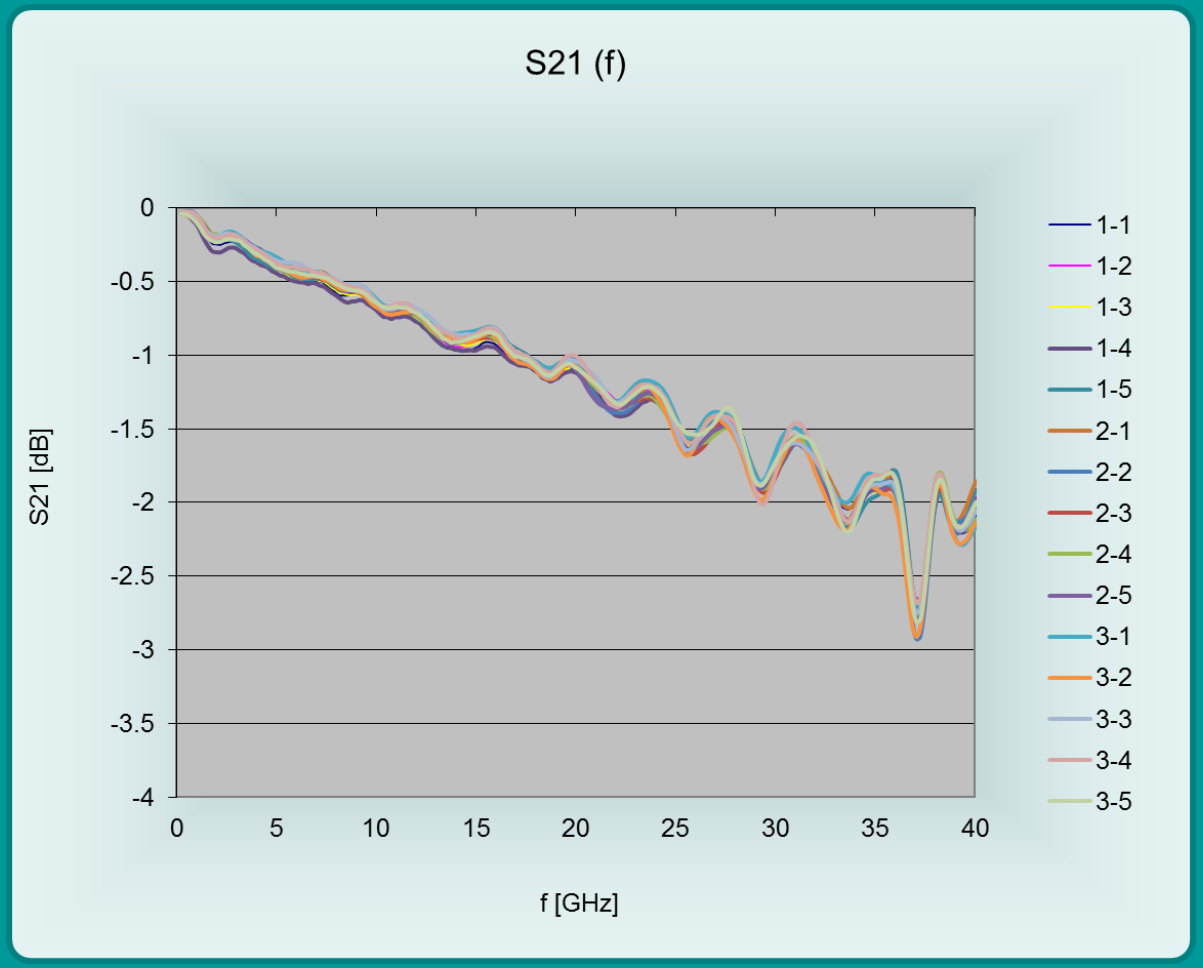
Insertion loss S21



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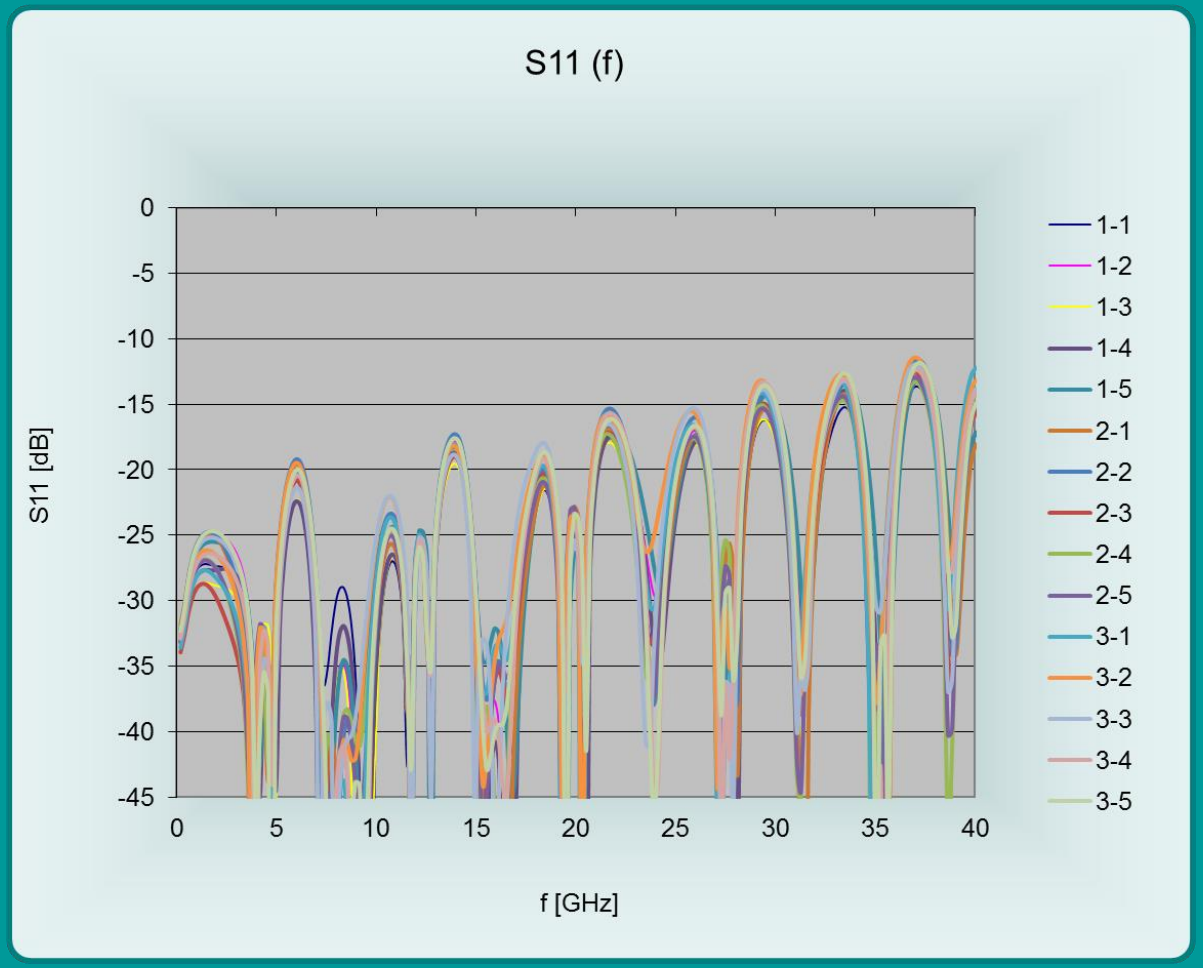
Return loss S11



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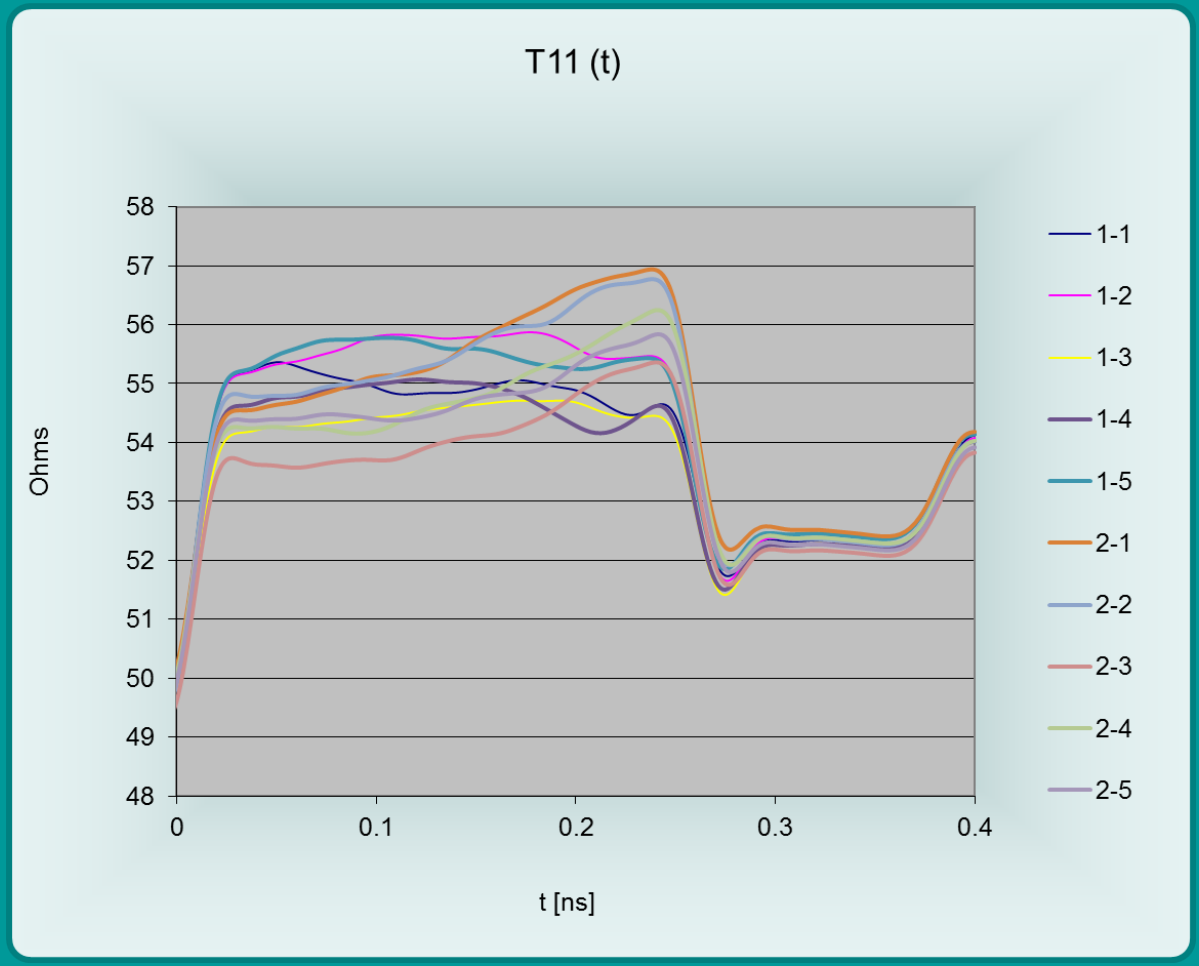
Time Domain Reflectometer



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Comments

- TDR slope is due to DC resistance of PCB trace
- When accounting for this, Zo of PCBs is ~52.5 Ohms
- TDR data board 3 fall into same band as boards 1 and 2
- They are, however, offset in time and thus excluded in graph

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